ABSTRACT OF THE DISCLOSURE

DC margin of a latch of a circuit under design is determined by performing three simulations. A simulation is performed to find the trip voltage of the forwarding inverter of the latch. A second simulation is performed to find the one margin of the latch. Lastly, a third simulation is performed to find the zero margin of the latch. During each of the simulations to find the one margin and the zero margin, the worst case input signal path from the various driver circuit elements and signal paths within the circuit under design is determined analytically by accumulating weighted resistance of each of the circuit elements along the signal paths. The weights assigned to the circuit elements are empirically determined based on the topology configuration of each of the circuit elements, e.g., the type circuit element, the signal being passed through the circuit element and whether a threshold voltage drop occurs between the drive circuit element and the pass circuit element.